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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/840,500	04/23/2001	Roger S. Tsai	12-1128	4458

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EXAMINER

STEVENS, THOMAS H

ART UNIT PAPER NUMBER

2123

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/840,500

Applicant(s)

TSAI, ROGER S.

Examiner

Thomas H. Stevens

Art Unit

2123

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 10 January 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-12 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |                                                                                                                                             |                                                                                         |
|---------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                                                                            | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                                        | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/6/02</u> . | 6) <input type="checkbox"/> Other: _____                                                |

**DETAILED ACTION**

1. Claims 1-12 were examined.

***Section I: Response to Applicant's Arguments***

***Drawings***

2. Applicants are thanked for addressing this issue. Based on applicant's response, objection is withdrawn.

***Information Disclosure Statement***

3. Applicants are thanked for addressing this issue. In light of applicant's response, the Japanese document (11330449) is now considered.

***Double Patenting***

4. Applicants are thanked for addressing this issue. The examiner is not in agreement with applicant's statement since examiner's reasoning was focused to the independent claims of the applications in question only. Rejection stands.

***35 USC § 102(b) and 103(a)***

5. Applicants are thanked for addressing this issue. The examiner is unfamiliar with applicant's phrase of "canned software"; nonetheless the prior art was mapped to parts of the claims in the first office action. Furthermore, applicants admitted that the prior art disclosed features related to the claims by stating that comparisons were made to experimental results and using test measurements (applicant's response: pg.5 of 6, 3<sup>rd</sup> paragraph, lines 3-6; and pg. 6 of 6, lines 4-5). Rejection stands.

***Section II: Rejections (Final Action, 2<sup>nd</sup> Office Action)***

6. Claim 1 of 09/840,500 is provisionally rejected under the judicially created doctrine of double patenting over claim 1 of application 09/840545. This is a provisional double patenting rejection since the conflicting claims have not yet been patented.

Claim 1 (09/840500) state a method of steps for modeling semiconductor devices: modeling device with a semi-physical model; modeling the semi-conductor device with an analytical thermal model; and coupling the semi-conductor device and analytical model; but does not specify which integral parts. Claims 1 (09/840545) disclose modeling a semiconductor device while detailing specific semiconductor parts.

One of ordinary skill in the art can deduce application 09/840500 is a broad representation of 09/840545 such that “fabricating”, “measuring”, “varying predetermined semiconductor devices” are processes identical to “modeling semiconductor devices”.

***Claim Rejections - 35 USC § 102***

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1-4, 7-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Biswas (“Modeling and Simulation of High Speed Interconnects” Dissertation (1998)). Biswas teaches increasing circuit density and improving transistor performance via simulation modeling.

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Claim 1. A method for modeling one or more predetermined characteristics of a semiconductor device comprising the steps (pg 39, section 4.1): a) fabricating a semiconductor device (pg. 3, lines 11-13), b) measuring one or more predetermined physical characteristics of said semiconductor device (pg. 6, section 2.4, lines 1-7); c) testing the semiconductor device (pg. 42, section 4.4 test chip); to establish a physically representative equivalent model of said one or more characteristics of said semiconductor device (pgs. 26-27, section 3.5.2 and pg. 30-31, section 3.5.4); d) varying one or more of said predetermined physical characteristics and fabricating a subsequent semiconductor device with said varied dimensions (pgs. 23-24, section 3.4.5) and e) testing of the sample to establish a correct said physically representative model (pg.40 with figure 4.1).

Claim 2. The method as recited in claim 1 (pg. 3, lines 11-13), further including the step of measuring the varied dimensions after said subsequent semiconductor is fabricated (pgs. 23-24, section 3.4.5).

Claim 3. The method as recited in claim 1 (pg. 3, lines 11-13), wherein a scanning electron microscope (SEM) is used to measure said predetermined dimensions in step (b) (pg. 48).

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Claim 4. The method as recited in claim 1(pg. 3, lines 11-13), wherein said testing in step (c) includes taking S-parameter measurements of said semiconductor device (pg. 51).

Claim 7. The method as recited in claim 1(pg. 3, lines 11-13), wherein said varied dimensions are measured by way of a SEM (pg. 48).

Claim 8. The method as recited in claim 1(pg. 3, lines 11-13), wherein said corrected physically representative model is corrected based upon S-parameter measurements (pg. 48).

Claim 9. A process for making a semiconductor device comprising the steps of: a) fabricating a semiconductor device (pg.3, lines 11-13); b) measuring one or more predetermined physical characteristics defining measured characteristics of said semiconductor device (pg.6, section 2.4, lines 1-7), c) testing said semiconductor device to establish a physically representative model (pg. 42, section 4.4 test chip); d) fabricating a subsequent semiconductor device in which said one or more measured characteristics are varied(pg.3, lines 11-13); deforming varied characteristics (pg.36) e) measuring said varied characteristics; and (pg. 36) f) testing said semiconductor device to establish a revised physically representative model of said semiconductor device (pg.40 with figure 4.1).

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Claim 10. The process as recited in Claim 9(pg.3, lines 11-13), further including step (g) repeating steps (d) through (9 one or more times.

Claim 11. The process as recited in claim 9(pg.3, lines 11-13), wherein said physically representative model in steps (c)(pg. 6, line 7) and (b) is based on predetermined S-parameter measurements (pg. 48).

Claim 12. The process as recited in claim 9(pg.3, lines 11-13), wherein steps (b) and (e) include measurement by way of a scanning electron microscope (pg. 48).

### ***Claim Rejections - 35 USC § 103***

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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11. Claims 5 and 6 are rejected under 35 U.S.C. 103 (a) as unpatentable by Biswas ("Modeling and Simulation of High Speed Interconnects" Dissertation (1998)), in view of VTT Electronics ("Research Activities in Microelectronics" (2000)). Biswas teaches increasing circuit density and improving transistor performance via simulation modeling; but doesn't teach scaling, biasing, or temperature variation. VTT Electronics teaches a series of nuances of semiconductor design, subsequently including temperature, bias, scaling and common source region analysis.

At the time the invention, it would have been obvious to one of ordinary skill in the art to use VTT electronics to modify Biswas since it would be advantageous to manipulate all features of the amplifier for full optimization.

Claim 5. The method as recited in claim 1(Biswas: pg. 3, lines 11-13), wherein said one or more predetermined characteristics include device scaling (VTT: pg. 8, line 10); bias dependence (VTT: pg. 6 Introduction, 3<sup>rd</sup> paragraph with figure 1); temperature dependence (pg. 26, Introduction) lay out dependence and process dependence.

Claim 6. The method as recited in claim 1(Biswas: pg. 3, lines 11-13), wherein said one or more predetermined physical characteristics include the physical dimensions of the source access region of said semiconductor device (VTT: pg. 8, 2<sup>nd</sup> paragraph).

### ***Conclusion***

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).



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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

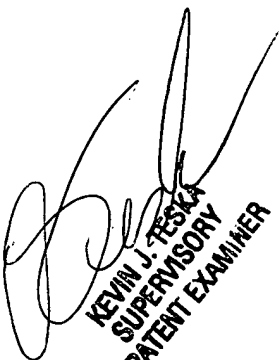
***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715, Monday-Friday (8:00 am- 4:30 pm) or contact Supervisor Mr. Kevin Teska at (571) 272-3716. Fax number is 571-273-3715.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

April 19, 2005

THS

  
KEVIN J. TESKA  
SUPERVISORY  
PATENT EXAMINER